III. REMARKS

Claims 1-24 and 31-36 are pending in this action. By this Amendment, claims 1, 9, 17, 31, 33 and 35 have been amended. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicants reserve the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the above amendments and following remarks is respectfully requested.

In the Office Action, claims 1-24 and 31-36 are rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Hall (US 5,936,868). Applicants respectfully submit that the claimed subject matter is allowable for the reasons that follow.

With respect to independent claims 1, 9, 17, 31, 33 and 35, Applicants submit that Hall does not disclose, *inter alia*, "identifying a scaling target for at least two problem objects of the design layout based on feedback from a manufacturing process regarding problems caused by the problem objects in manufacturing an integrated circuit chip according to the design layout[.]" (Claim 1, similarly claimed in claims 9, 17, 31, 33 and 35). Hall only discloses "converting an original IC design for an original manufacturing process to an updated IC design for an updated manufacturing process" (col. 3, lines 34-36), but does not disclose feedback regarding problems caused by any component of the original IC design in manufacturing an integrated circuit according to the original IC design. Hall upgrades the original IC design, but does not upgrade it based on a problem in manufacturing the IC caused by a problem object in the original IC design. In addition, Hall does not disclose identifying "problem objects". The Office asserts that "at least two problem objects are necessarily identified for which the scaling are applied[.]"

(Office Action at page 3, emphasis added). Applicants respectfully disagree because Hall does not necessarily identify "problem objects" for the scaling. Hall identifies particular types of components, e.g., vias, supply rails, etc., to scale, but not an individual "problem object" that causes a problem in manufacturing. In addition, note that a target object for the scaling in Hall is not necessarily a "problem object" which causes a problem in manufacturing. The target objects are simply types of structure in Hall. In view of the foregoing, Hall does not disclose the above features. Accordingly, Applicants respectfully request the Office withdraw the rejection.

In addition, Hall does not disclose, *inter alia*, "individually determining a scaling factor for each problem object without considering a scale factor of a different problem object of the same type as the problem object[.]" (Claim 1, similarly in claims 9, 17, 31, 33 and 35). In Hall, components of the same type are scaled using the same scale factor. That is, for example, all vias are scaled using the same scaling factor; all polysilicon gates are scaled using the same scaling factor; and all power supply rails are scaled using the same scaling factor in Hall. (*See*, col. 4, lines 1-40.) Hall does not disclose individually determining a scaling factor for each (individual) component because Hall considers the scaling of all other componnets of the same type.

Moreover, Hall does not disclose, *inter alia*, "determining which at least one of a plurality of scaling techniques is to be applied to each problem object[.]" Hall only discloses downsizing or upsizing a structure, which are only goals or result (or directions) of scaling, but not scaling techniques to achieve the goals/results. The division of one elongate contact into a plurality of generally square contacts is also a goal or a result of scaling, but not a scaling technique. In contrast, the current application provides flat scaling, minimum perturbation compaction, and scaling of custom circuitry as examples of scaling techniques, which are all

techniques to achieve the claimed scaling. (*See*, e.g., para. 38-45 of the current application.) Applicants respectfully submit that it is illogical to equate a goal such as upsizing (make bigger) and downsizing (make smaller) with a technique to achieve the goal. Hall simply does not disclose a scaling technique, and does not disclose determining a scaling technique to be applied to each problem object.

In addition, with respect to claims 31, 33 and 35, Hall does not disclose that "the scaling factor includes at least one of a compensation and a new ground rule." (Claim 31, similarly claimed in claims 33 and 35). Hall only discloses scaling a component in an IC (col. 4, lines 1-2) and/or dividing an elongate contact into multiple generally square contacts (col. 4, lines 16-19), but does not include a compensation or a new ground rule. In the Office Action, the Office asserts that Hall includes this feature, but the cited disclosure of Hall (col. 3, line 30 to col. 4, line 67), and/or the Hall disclosure as a whole, does not provide any support for the assertion. In view of the foregoing, Hall does not anticipate claims 31, 33 and 35. Accordingly, Applicants respectfully request withdrawal of the rejection.

Applicants respectfully submit that the application is in condition for allowance. Should the Examiner believe that anything further is necessary to place the application in better condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

/ Spencer K. Warnick /

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